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# **Multi-Channel Transcutaneous Cortical Stimulation System**

**Contract # N01-NS-7-2365**

**Progress Report #5**

**for the contract period 4/1/98 – 6/30/98**

**Illinois Institute of Technology**

**Principal Investigator: Philip R. Troyk, Ph.D.**

## Introduction

The goal of this project is the design, fabrication, and testing of a *Multi-Channel Transcutaneous Cortical Stimulation System* to be used in a prototype artificial vision system. During the past 25 years, the development of a neuroprosthesis which could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This project uses the combined capability four organizations, the Illinois Institute of Technology, P.I. Medical, Cross Technology, and the A.E. Mann Foundation to accomplish this challenging task.

This is the fifth progress report for this project. In this report we describe our progress on the ceramic package for the 64-channel submodules and our progress on the ASIC designs.

## Progress on Design of the Implant Package

In our fourth progress report we reported that we were investigating the use of a class of new ceramic adhesives, manufactured by Cotronics Inc. The adhesives are 100% inorganic and are commonly used for sealing vacuum electronic assemblies such as light bulbs and ceramic vacuum furnaces. They are based upon low-temperature sintering of Aluminum Oxide through the use of magnesium oxide activators. Theoretically, it should be possible to achieve over 99% density. And, they met our requirements of a low processing temperature of less than 350 degrees C.

We obtained some of these adhesives and performed laboratory testing of ceramic layers bonded together. The initial testing consisted of immersion in boiling water for an extended period of time for examination of its bonding capabilities. These tests showed exceptional bonding capabilities which remained even after a month in boiling water.

We then proceed to test these materials for sealing hermetic packages. We used glass microscope slides for our initial testing. Use of the slides allowed us to fabricate numerous test packages very quickly. The ability to view the interior of the packages was a major advantage. We also ~~placed~~ submersed the packages under water with food dye, while we pulled a vacuum. Following the vacuum test, some of which lasted for 2 days, we could then examine the interior of the package for water content, as well as determine the physical condition of the seal area under 200x power. This crude leak test allowed us to make rapid progress in accessing the feasibility of using these adhesives. Several dozen samples were made using a variety of deposition, drying, and sintering techniques.

Although we were able to achieve packages which passed our "vacuum-water" test and showed no evidence of water penetration into the packages, the process was not readily repeatable. At the assembly step of sealing, the implant packages will have a considerable investment in assembly time and material costs. Therefore we need a sealing process which has a high degree of repeatability. After exhaustive testing we decided that the sintered ceramics would not have the requisite reliability to act as the primary seal for the visual prosthesis.

However, we do see a possibility for their use as adhesives in other locations in the implant package.

We then shifted our focus to investigating glass seals which we could process at IIT.

We have obtained sample sheets of the Macor and plan to use it as the ceramic material for the submodule package. This decision is based upon our tests in which we were able to machine very intricate patterns using a sophisticated NC mill. All of the features required by our design are easily machined directly from our CAD drawings. Using the Macor has eliminated major concerns associated with the laser machining of the aluminum oxide.

To accomplish the glass to ceramic seals, we contracted to have a low-temperature glass formulated to match the temperature coefficient of the Macor. We have obtained two different samples of candidate glasses and proceeded to use our glass microscope slide method to investigate the quality of the seals. We outfitted our lab with suitable furnaces and processing equipment, and fabricated prototype glass packages.

Our initial results are quite promising and far superior to the sintered ceramic packages. Within only 2 days, we were able to repeatedly seal packages which passed our vacuum/water tests. We immediately proceeded to investigate the survival of the glass seals in extended 95° C saline soak tests. We will continue developing the techniques for the glass seals during the next quarter. We plan to be able to send sealed ceramic packages to the Mann Foundation for rigorous helium leak testing.

We have also started evaluating the Macor for its suitability for deposition of metal. Electrofilms is continuing with their fabrication of the masks for the prototype submodule packages, and Cross Technology is preparing Macor samples with metal deposited on the edge. These edge-deposited samples will be sent to P.I. Medical for the development of the laser schedules needed to pattern the electrode contacts.

## **Progress on the design and fabrication of the submodule ASICs.**

During the past quarter we have fabricated and partially tested MOS9, and submitted two new ASICs, BLOCK1 and BLOCK2 for fabrication. The designs, simulations, and layouts, were performed at IIT. Fabrication was accomplished by AMI through the MOSIS fabrication service.

### **Testing of MOS9**

During the last quarter we had identified an anodic/cathodic balance problem in DAC6 which we believed was associated with impact ionization of the output driver transistors. We had revised our DAC design using extremely conservative guarding of the DAC reference mirrors to eliminate this effect. This new design was contained in MOS9, which we described in our last report.

This quarter we received MOS9 back from the foundry and began our testing. Unfortunately, MOS9 arrived a couple of days before we were scheduled to send off a new DAC design, described below. Therefore we do not have complete test data to report. However, we were able to verify that the original impact ionization problem had been significantly improved,

although a remaining problem which involved ranging among the three groups of DAC bits was now exposed. Although anodic/cathodic tracking was closer to our expectations, the currents did not scale as expected when shifting from one set of bits to another.

We theorize that this effect is also due to impact ionization, but in a different circuit location. Our reference generator/chain design has minor, but important operating point differences between the fundamental reference stage and the subsequent chain stages which set the values of the individual bits. We have modified the reference chain to use extended-drain transistors in cascode configurations at these critical locations. This change was included in a new submission during this period and we will be able to verify its effectiveness during the next quarter.

### **Technology Shift to AMI native rules**

During this quarter we made a major change to our layout technology. Previously we had been submitting all of our ASIC designs in what are called "Scaleable CMOS rules", or "MOSIS rules". This rule set allows for rapid device layout due to the simplicity of the rule set. In our earlier designs, this simpler rule set was not a limitation to our ASIC investigations. However, we had always intended to change to "AMI native rules" once the feasibility of our circuit designs was established.

During this quarter we have made the technology shift to native rules. Ultimately we need to layout all designs in native rules so that we can procure full wafer runs directly from AMI, since the cost of doing so will be significantly reduced below the costs which we would incur through MOSIS. Fortunately we can use the native rules in our continuing prototype work through MOSIS. It took about one month of effort for us to make the native rule shift. However, now that the technology file has been developed, all future designs will be fabricated in native rules.

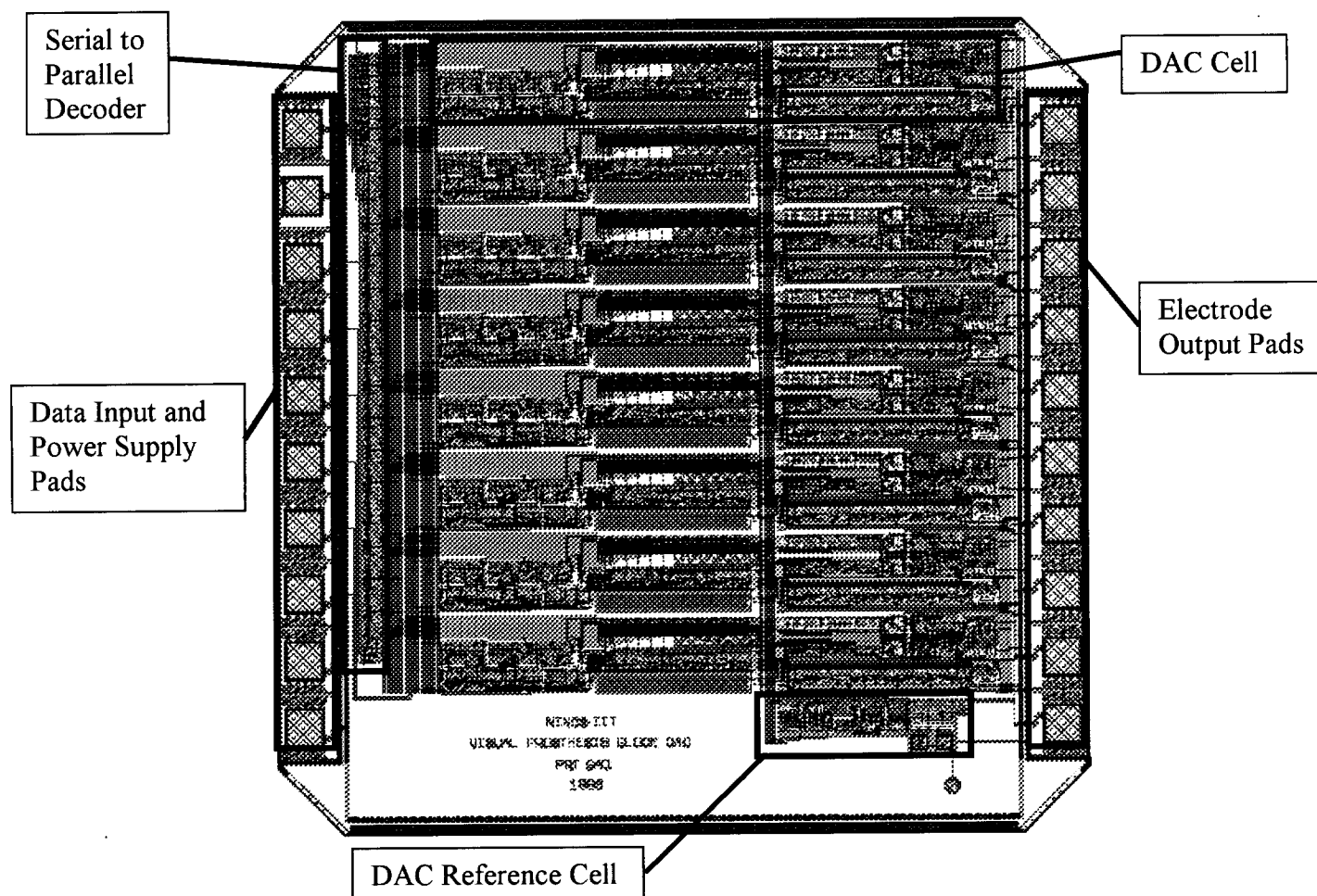
### **Design of Block1 and Block2**

Following the shift to native rules we proceeded to revise our DAC design in this new rule set. We also designed our first version of the 8-channel BLOCK chip which will form the heart of our implant output stages. The BLOCK chip is designed to be a serial-in/analog-out ASIC. The chip will contain 8 channels of DAC cells, each with their own storage for amplitude information, and pulse-width timing. One reference cell will be used for all 8 channels. A serial-to-parallel decoder will drive a common data buss for controlling and commanding each of the channels. 8 of these BLOCK chips will be used in each implant submodule to obtain 64 channels per submodule.

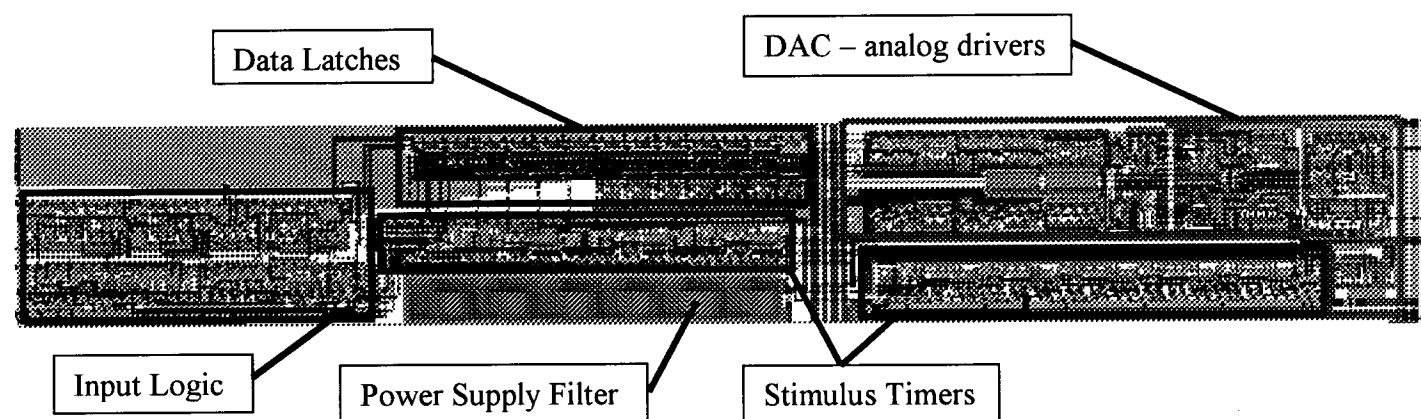
Figure 1, below, shows the layout of BLOCK1. BLOCK1 is a complete serial-in to electrode-driver-out, 8 channel chip. The data protocol used for the serial data is compatible with the overall data protocol of the visual prosthesis system. In Figure 2, below, an individual DAC cell is shown. Outlined are the various circuit stages.

After receipt of MOS9, we quickly revised BLOCK1 to another design BLOCK2. BLOCK2 uses the extended drain transistors to address the issue of bit tracking, described above. Both BLOCK1 and BLOCK2 were submitted for fabrication and we expect to receive them during the next quarter.

The only element missing from BLOCK1 and BLOCK2 is the analog-to-digital converter for monitoring the electrode voltages. We intend to produce our first AD converter design and submit it for fabrication next quarter.



**Figure 1 – Layout of BLOCK1**



**Figure 2 – Layout of DAC cell from BLOCK1 and BLOCK2**